

CAT33C204

4K BIT SERIAL E²PROM

3VOLT

OPERATION

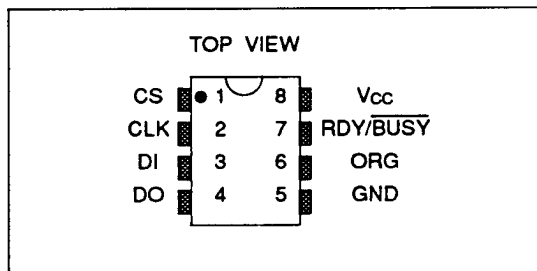
DESCRIPTION

The CAT33C204 is a 4K bit Serial E²PROM memory device organized in 256 registers of 16 bits (ORG pin at V_{cc}) or 512 registers of 8 bits each (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT33C204 is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 10,000 erase/write cycles and has a data retention of 10 years. It is packaged in an 8-pin DIP and Small Outline packages. It is also available in a 5V version (CAT35C204).

FEATURES

- Compatible with General Instruments ER5912
- Single 3V supply
- 256x16 or 512x8 user selectable serial memory
- 20ms programming cycle
- Self timed programming cycle with Autoerase
- Highly reliable CMOS floating gate technology
- Word and chip erasable
- Operating range 0°C to +70°C [Industrial temp. range available]
- 10,000 erase/write cycles
- 10 year data retention
- Power-up inadvertent write protection

PIN CONFIGURATION

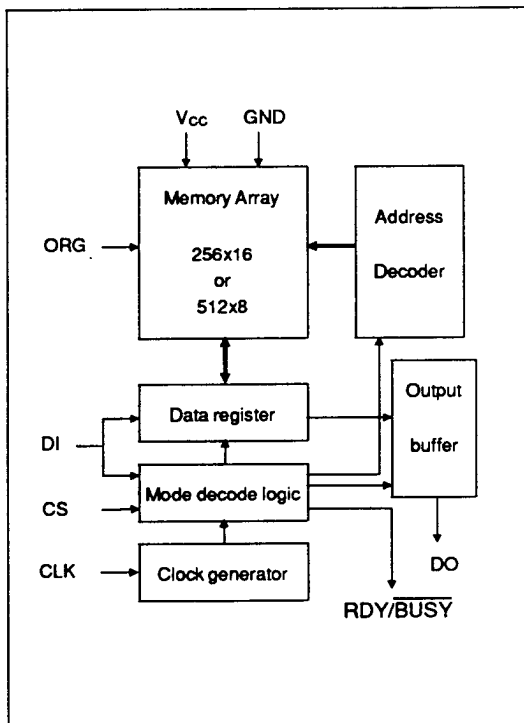


PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
V_{cc}	+5V power supply
RDY/BUSY	Status output
GND	Ground
ORG	Memory organization

Note: When the ORG pin is connected to V_{cc}, the 256x16 organization is selected. When it is connected to ground, the 512x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 256x16 organization.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Storage temperature	-65°C to +150°C
Power supply (V _{CC})	+7V
Voltage on any input pin	-0.3 to +7V
Voltage on any output pin	-0.3V to V _{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +3V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I _{CC1}	Current consumption	V _{CC} =3.0V, CS=3.0V, DI=0.0V SK=3.0V, DO Unloaded			2.0	mA
					0.5	
I _{CC2}	Current consumption (stand-by)	V _{CC} = 3.3V, CS = 0V DI = 0V, SK = 0V			50	µA
I _{LI}	Input leakage current	V _{IN} = V _{CC} +0.1V			10	µA
I _{LO}	Output leakage current	V _{OUT} = V _{CC} , CS = 0			10	µA
V _{IH}	High level input voltage		V _{CC} -0.3		V _{CC} +1	V
V _{IL}	Low level input voltage		-0.1		0.3	V
V _{OH}	High level output voltage	I _{OH} = -10µA	V _{CC} -0.3			V
V _{OL}	Low level output voltage	I _{OL} = 10µA			0.3	V

INSTRUCTION SET

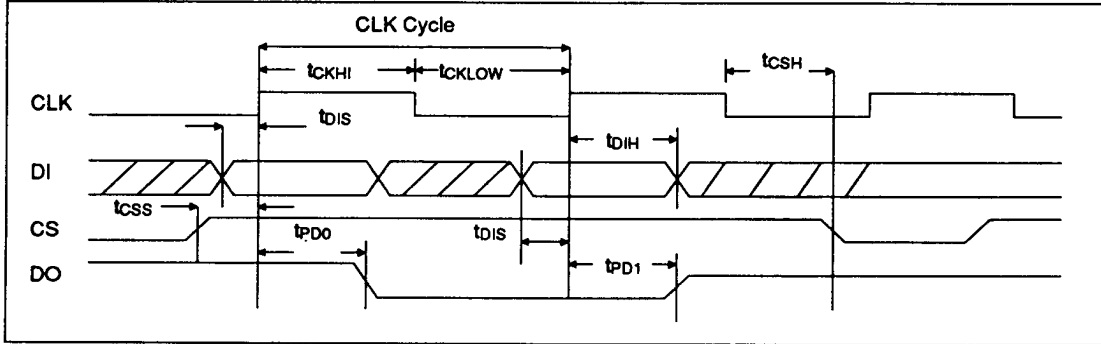
Instruction	Start Bit	Opcode	Address		Data		Comments
			512 x 8	256 x 16	512 x 8	256 x 16	
READ	1	1000	A8 - A0	A7 - A0			Read address AN - A0
PROGRAM	1	X100	A8 - A0	A7 - A0	D7 - D0	D15 - D0	Program address AN - A0
PEN	1	0011	00000000	00000000			Program enable
PDS	1	0000	00000000	00000000			Program disable
ERAL	1	0010	00000000	00000000			Erase all addresses
WRAL	1	0001	00000000	00000000	D7 - D0	D15 - D0	Write all addresses

AC CHARACTERISTICS(V_{CC} = +3V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
t _{CSS}	CS setup time		0.2			μs
t _{CSH}	CS hold time	C _L = 100pF See Note 1. below	0			μs
t _{DIS}	DI setup time		0.4			μs
t _{DIH}	DI hold time		0.4			μs
t _{PD1}	Output delay to 1				2	μs
t _{PD0}	Output delay to 0				2	μs
t _{EW}	Erase/Write pulse width				20	ms
t _{SKHI}	Minimum SK high time		1			μs
t _{SKLOW}	Minumun SK low time		1			μs
CK _{MAX}	Maximum frequency		DC		250	KHz

Note 1. All timing measurements on the CAT33C204 are defined at the point of signal crossing V_{CC} + 2.

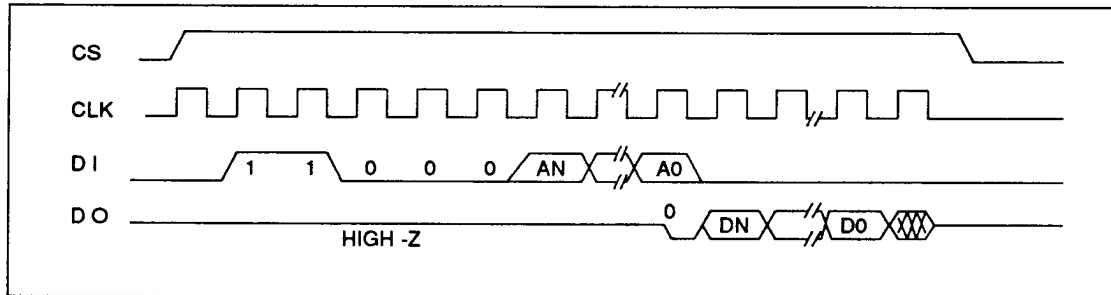
SYNCHRONOUS TIMINGS



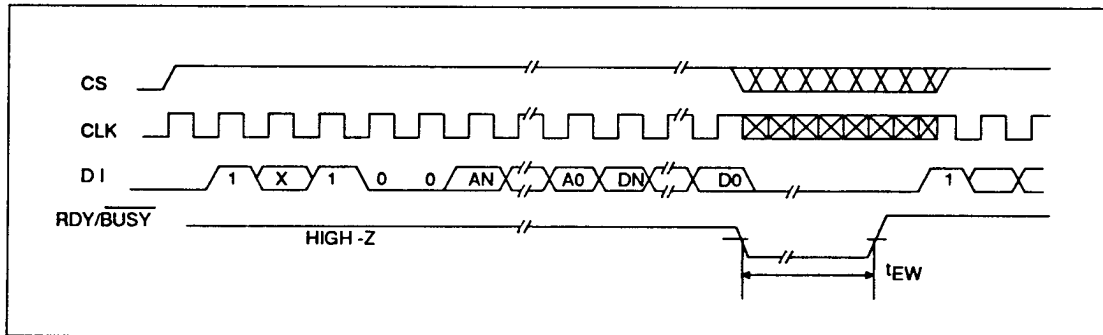
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or A_N)	D_N (or D_N)
512 x 8	A_8	D_7
256 x 16	A_7	D_{15}

INSTRUCTION TIMING <READ>



INSTRUCTION TIMING <PROGRAM>



CAT33C204 is one logical "1" start bit, a 4 bit op code, an 8 bit address (9 bit address when organized as 512 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 512 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT33C204 will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and becomes stable after the specified time delay (t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT33C204 powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS

instruction can be used to disable all the CAT33C204's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT33C204 regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/ $\overline{\text{BUSY}}$ pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C204 can be determined by polling the RDY/ $\overline{\text{BUSY}}$ pin.

ERASE ALL

Upon receiving an ERAL command, the RDY/ $\overline{\text{BUSY}}$ pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT33C204 can be determined by polling the RDY/ $\overline{\text{BUSY}}$ pin. Once erased, all memory bits return to logical "1" state.