Preliminary data

Type	Ordering code	Package
SDA 2116	Q67100-A2128	DIP 8

Features

- Word-organized programmable nonvolatile memory in n-channel floating-gate technology
- 128 x 8 bit organization
- Supply voltage 5 V, programming voltage 24 V
- A total of 3 lines provides data transfer and chip control between processing unit and E²PROM
- Data (8 bits), address (7 bits) and control information input (1 bit) as well as serial data output
- More than 10^3 reprogramming cycles per address
- Data retention in excess of 10 years (within specified operating temperature range)
- Unlimited number of reads without refresh
- Erase and write cycle in 50 ms each

Maximum ratings

Supply voltage 1 range	V_{CC}	−0.3 to 6	V
Supply voltage 2 range	V_{PP}	−0.3 to 26	V
Input voltage range	V_i	−0.3 to 6	V
Power dissipation	P_V	75	mW
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	100	K/W

Operating range

Supply voltage	V_{CC}	4.5 to 5.5	V
Ambient temperature	T_A	0 to 70	°C

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Static characteristics

		min	typ	max	
Supply voltage 1	V_{CC}	4.5	5	5.5	V
Supply current 1	I_{CC}			5	mA
Supply voltage 2	V_{PP}	22.8[1]	24[1]	25.6[1]	V
Supply current 2	I_{PP}			2	mA
Inputs					
(D, Φ, $\overline{CE}$)	V_L			0.5	V
$V_H = 5.5$ V	V_H	3.0			V
	I_H			10	µA
Data output D (open drain)					
$V_L = 0.5$ V	I_L			0.5	mA
$V_H = 5.5$ V	I_H			10	µA
Clock pulse Φ					
High duration	Φ_H	2.5		60	µs
Low duration					
before/after Φ_H	Φ_L	5			µs
before/after $\overline{CE}$ transition	Φ_L	5			µs
before/after D change	Φ_L	2.5			µs
Data D					
before/after Φ trailing edge	D_H	2.5			µs
	D_L	2.5			µs
Time between rising and trailing edge					
$\overline{CE}$ referenced to D	Δt	2.5			µs
Erase time	t_{er}	50		100	ms
Write time	t_{wr}	50		100	ms

1) Voltage peaks higher than the static value of V_{PP} must be avoided, e.g. by a Z diode between the inputs 6 and 1.

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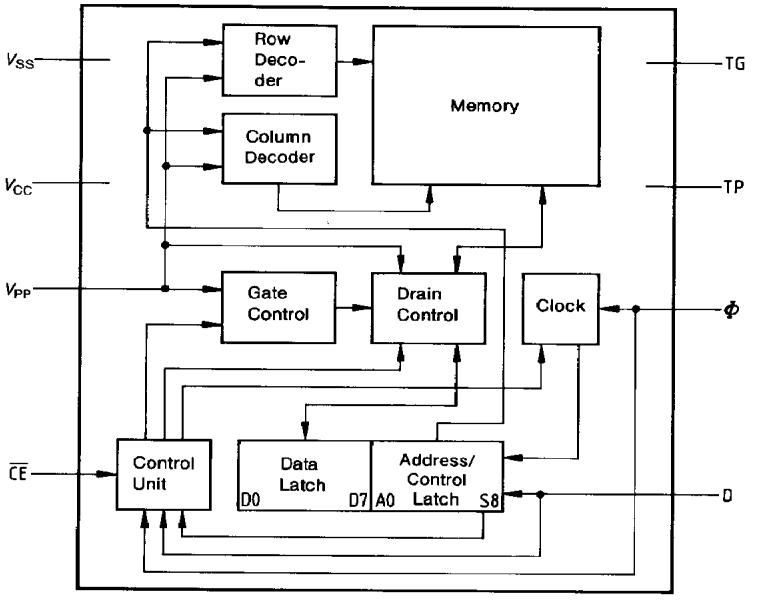
Block diagram



Pin description

Pin	Symbol	Function
1	V_{SS}	GND
2	$\overline{CE}$	Chip enable
3	V_{CC}	Supply voltage 5 V
4	D	Data input/output
5	Φ	Clock input
6	V_{PP}	Programming voltage 24 V
7	TP	Test input, to V_{SS}
8	TG	Test input, remains open

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Data transfer and chip control

Total data transfer between processing unit and E²PROM memory requires 3 lines, each of which has several functions.

a) Data line D:
- bidirectional serial data transfer
- serial address input
- clocked input of control information
- direct control input

b) Clock line Φ:
- data, address and control bit input
- data output
- start data output with data transfer from memory into the shift register, or start data change when reprogramming.

c) Chip enable line $\overline{CE}$:
- chip reset and data input (active high)
- chip activating (active low)

The data address and control information is clocked into the chip before the chip is enabled. This data remains stored in the shift register during reprogramming and reading, until the second clock pulse has been received.

The following data must be applied:

a) Memory read: One 8-bit control word comprising
- 7 address bits A0 to A6 (A0 as LSB first)
- 1 control bit, SB = "0", after A6

b) Memory change (Erase and/or write)
16 bits input information comprising
- 8 bits, D0 to D7, is new memory information (D0 as LSB first)
- 7 bits, A0 to A6, is address information (A0 as LSB after D7 first)
- 1 bit is control information, SB = "1", after A6

Read (figure 1)

After the negative edge of $\overline{CE}$ and the data input is received, the read operation starts through the selected word address when SB = "0".

With the first clock pulse after $\overline{CE}$ = "0", the data word is transferred out of the selected memory address into the shift register. After the first Φ-pulse has been terminated, the data output becomes low in impedance and the first data bit D0 can be read. With each following clock pulse, a further data bit will be passed on to the output. The data line again turns high in impedance after the positive edge of $\overline{CE}$.

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Reprogramming (figure 2)

A complete reprogramming operation normally consists of an erase cycle and a following write cycle. During erase every bit of the selected word will become "1" and during write each bit of the word becomes "0" according to the information in the shift register.

After the chip has received the data and then been enabled, reprogramming starts if SB = "1" is present in the relevant cell of the shift register. Whether an erase or write cycle is triggered, depends on the information of the data line D during chip activation.

Erasing a word into the "1"-status requires a "1" at the data input during the negative edge $\overline{CE}$. Should, however, a write cycle into "0"-status be started, then a "0" must be on the data line during negative edge of $\overline{CE}$.

To start programming a start pulse must be applied to clock input Φ, and the control information at D must remain stable until its positive edge is received. The active data change starts with the trailing edge of this start pulse. The programming cycle will be terminated by a reset of the chip enable; e.g. by applying $\overline{CE}$ = "1".

The reprogramming of a word begins with the erase procedure. $\overline{CE}$ = "1" ends the erase cycle. The control bit in the shift register SB = "1", which is also required for the write cycle, remains stable even after termination of erase cycle. In order to write the selected word, the data line D must be switched from "1" to "0", the chip must again be activated with $\overline{CE}$ = "0" and with the aid of a start pulse, the data change can be started.

Erase and write can, of course, also be done separately. To obtain a stable "1" in all 8 bits of the selected memory address during erasing, a data word with all bits "1" must be read in before the erasing process begins. If data is written into a previously not erased memory word the "0" status of the old and the new information will be added.

Reset and supply voltages

A non-addressed memory automatically remains in reset position through $\overline{CE}$ = "1". All flipflops in the process control section are reset. The information in the shift register, however, remains stable and will only be changed by shifting data.

If it is not possible to ensure a defined position for the signal states (quiescent state $\overline{CE}$ = high, Φ = low) during switch-on and switch-off of the supply voltages, data loss occuring during unintentional decoding-out of program instructions can be avoided by enabling V_{PP} after V_{CC} and disabling it before V_{CC}.

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Read cycle (1-Kbit E²PROM)

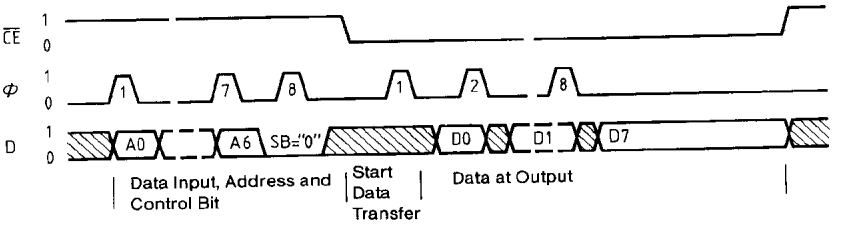

Figure 1

Reprogramming cycle (1-Kbit E²PROM)

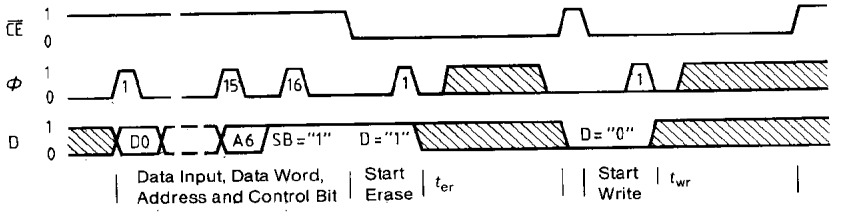

Figure 2

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