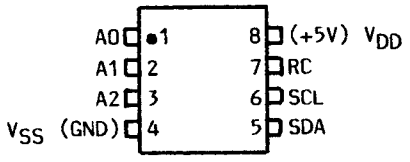
1024 BIT SERIAL ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

FEATURES:

- 256 x 8 serial EEPROM
- Single +5V only operation
- Compatible with the inter-integrated-circuit (I^2C) bus
- Fully TTL compatible inputs and outputs
- Unlimited read accesses
- ESD Protection: Inputs are designed to meet 1.0KV per test method 3015.1, MIL-STD 883
- Highly reliable N-Channel SNOS technology
- Designed for 10 year data retention after 10,000 erase/write cycles per word
- 0°C to +70°C operating ambient temperature range

PIN CONFIGURATION
8 LEAD DUAL IN LINE

TOP VIEW

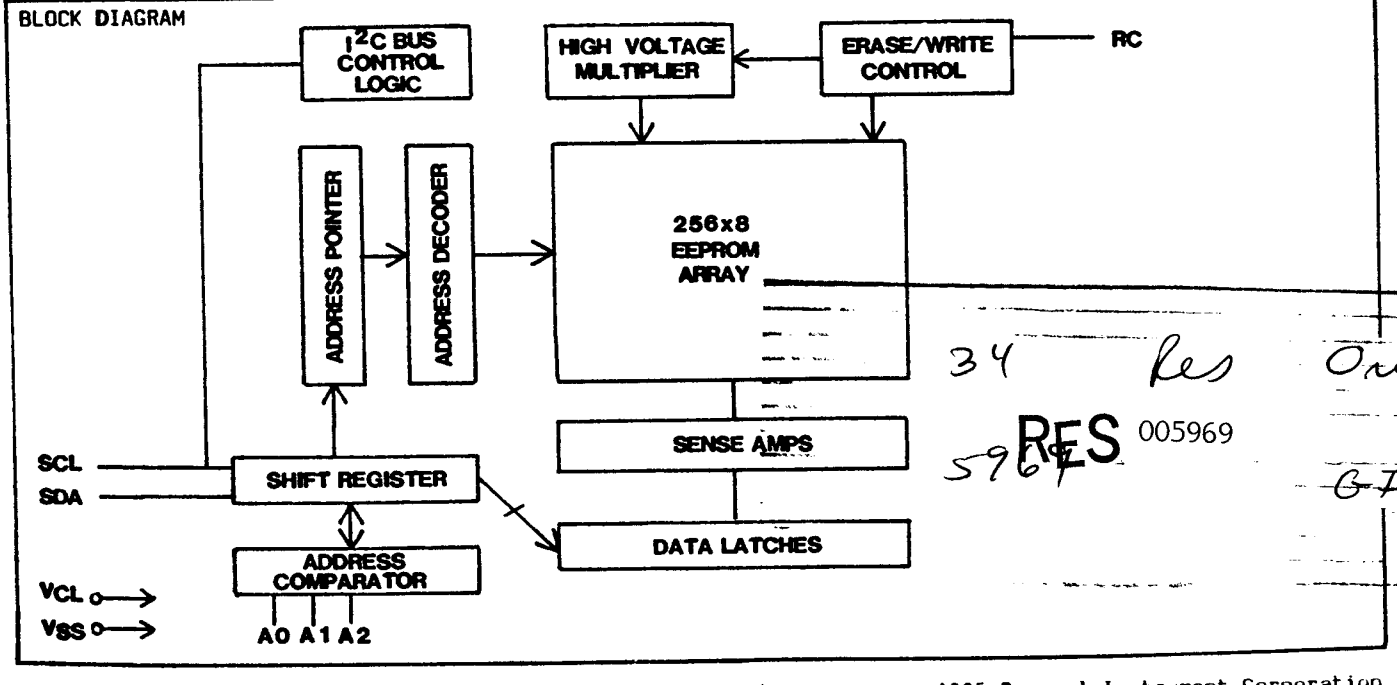


DESCRIPTION

The PCD8582 is a 2K EEPROM manufactured in General Instrument's highly reliable SNOS technology. The key features of this device are its +5 volt only operation and inter-integrated circuit (I^2C) bus compatibility. This revolutionary bus provides the facilities of a local area network within a single system or equipment. Each IC serves as both transmitter and receiver in the synchronous data transfer of up to 100K bits per second. The use of I^2C compatible devices make possible modular circuit design with up to 600 feet of separation allowable between IC's (400 pf maximum bus capacitance).

Chip select is accomplished by means of the three address inputs A0, A1 and A2. Each of these inputs must be connected externally to either +5V or GND and each chip is then selected through software by placing its 3 bit chip select address on the serial data input line (SDA) at the appropriate time in the bus protocol. Up to eight PCD8582s may be connected to the I^2C bus.

BLOCK DIAGRAM



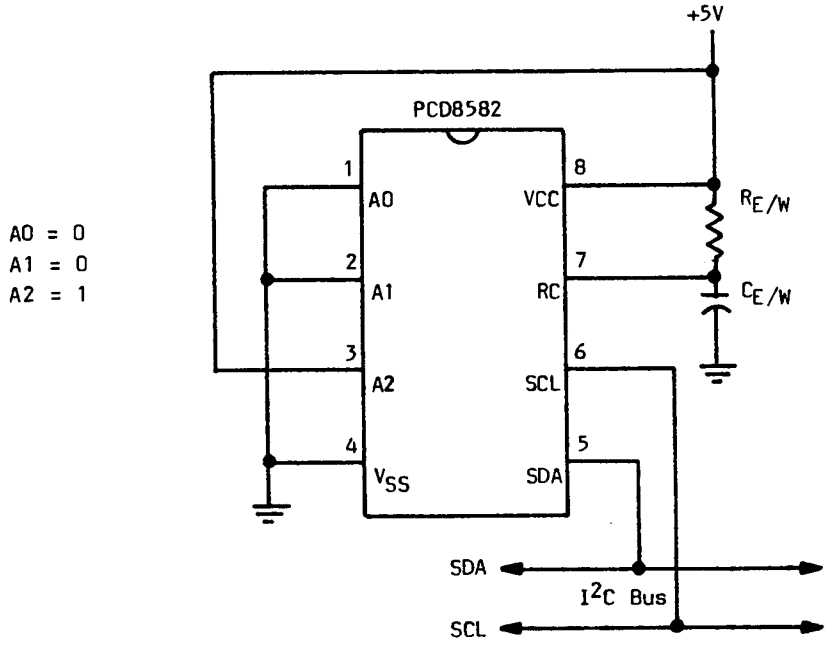
PIN FUNCTIONS

A0, A1, A2	Chip Address Inputs
V_{SS}	Ground
SDA	Serial Data/Address, Input/Output
SCL	Serial Clock Input, Erase/Write
RC	Time Constant Network Input
V_{DD}	+5V Power Supply

Figure 1 below shows the typical manner in which the PCD8582 is interfaced to the I^2C bus. For purposes of illustration chip address A2A1A0 = 100 is shown. This is only one of eight possible addresses since up to eight PCD8582s can be connected to the I^2C bus of a single system. The erase/write cycle time of this device $T_{E/W}$ is determined by an external resistor and capacitor: $R_{E/W}$ and $C_{E/W}$.

NOTE:
When the PCD8582 is not used in an I^2C bus configuration, pull-up resistors for SDA and SCL are required.

FIGURE 1 TYPICAL INTERFACE



DS20025A-2

CHARACTERISTICS OF THE I^2C BUS

The I^2C bus is intended for communication between different ICs. This serial bus consists of two bi-directional lines: one for data signals (SDA) and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pullup resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus not busy: Both data and clock lines remain HIGH.

Start data transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines the START condition.

Stop data transfer: A change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the STOP condition.

Data valid: The state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE + WRITE mode and is not limited in the READ mode. The information is transmitted bytewise and each reciever acknowledges with a nineth bit which must be provided by the user.

Within the I^2C bus specifications a low speed mode (2 KHz clock rate) and a high speed mode (100 KHz clock rate) are defined. The PCD8582 works in both modes. By definition a device that gives out a message is called "transmitter", the receiving device that controls the message is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves".

Acknowledge: Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the high period of the acknowledge related clock pulse. Of course setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line HIGH to enable the master to generate the STOP condition.

ELECTRICAL CHARACTERISTICS

Standard Conditions (unless otherwise noted)

V_{SS} = 0V (GND)
V_{DD} = +5 ± 10% volts
Ambient Operating Temperature (T_A):
0°C to +70°C (Commercial)

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

General Instrument makes no warranty, expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software supplied to the customer.

*ABSOLUTE MAXIMUM RATINGS

Characteristic	Sym	Min	Typ	Max	Units
Power Supply Voltage	V_{DD}	-0.3	-	7.0	V
Voltage On Any Input Pin	V_I	V_{SS}-0.8	-	V_{DD}+0.8	V
Ambient Operating Temperature	T_A	0	-	+70	°C
Storage Temperature (Unpowered and without data retention)	T_{STG}	-65	-	+150	°C
Current Into Any Input Pin	I_I	-	-	100	µA
Output Current	I_O	-	-	3	mA (SINK)
Soldering Temperature of Leads (10 seconds)	-	-	-	300	°C

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Operating Supply Current READ Mode	I_{DDR}	-	15	-	mA	
Operating Supply Current WRITE/ERASE Mode	I_{DDW}	-	15	-	mA	
Operating Supply Current STANDBY Mode	I_{DDO}	-	12	-	mA	
Input Leakage Current (A0, A1, A2, SCL Pins)	I_{IL}	-	-	1	µA	
Output Leakage Current HIGH	I_{OH}	-	-	1	µA	
SCL Input and SDA Input/ Output Pins:						
High Level Input Voltage	V_{IH}	3.0	-	V_{DD}+0.8	V	
Low Level Input Voltage	V_{IL}	-0.3	-	1.5	V	
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 3mA V_{DD} = 4.5V
A0, A1, A2 Pins:						
High Level Input Voltage	V_{IH}	V_{DD}-0.5	-	V_{DD}+0.5	V	
Low Level Input Voltage	V_{IL}	-0.3	-	0.5	V	

ELECTRICAL CHARACTERISTICS

AC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Units	Conditions
SCL Clock Frequency	f_{SCL}	0	-	100	KHz	
The LOW period of the clock	t_{LOW}	4.7	-	-	µs	
The HIGH period of the clock	t_{HIGH}	4.0	-	-	µs	
SDA and SCL rise time	t_R	-	-	1	µs	
SDA and SCL fall time	t_F	-	-	300	ns	
START condition hold time. After this period the first clock pulse is generated.	$t_{HD;STA}$	4.0	-	-	µs	
Setup time for start condition (Only relevant for a repeated start condition)	$t_{SU;STA}$	4.7	-	-	µs	
Data set-up time	$t_{SU;DAT}$	250	-	-	ns	
Data hold time for I^2C devices	$t_{HD;DAT}$	0	-	-	µs	See note 2
STOP condition set-up time	$t_{SU;STO}$	4.7	-	-	µs	
Time the bus must be free before a new transmission can start	t_{BUF}	4.7	-	-	µs	
Erase/Write Cycle Time (per word)	$T_{E/W}$	20	30	100	ms	C=2500pf, R=10K
Endurance (Number of erase/ write cycles)	$N_{E/W}$	-	-	10,000	E/W cycles	Per byte
Data Retention Time	t_S	10	-	-	Years	
Input Capacitance on SCL, SDA	C_I	-	-	7	pf	
Noise Suppression Time Constant at SCL and SDA input	T_I	0.25	0.5	1.0	µs	

NOTES:
1. All values referred to V_{IH} and V_{IL} levels.
2. Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300ns) of the falling edge of SCL.

FIGURE 2A DATA TRANSFER SEQUENCE ON THE SERIAL BUS

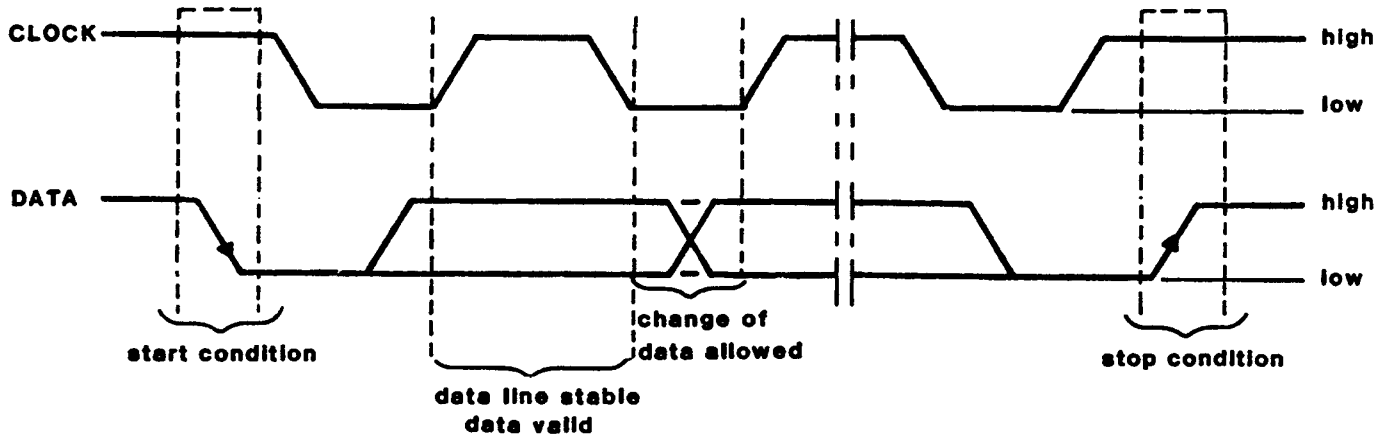
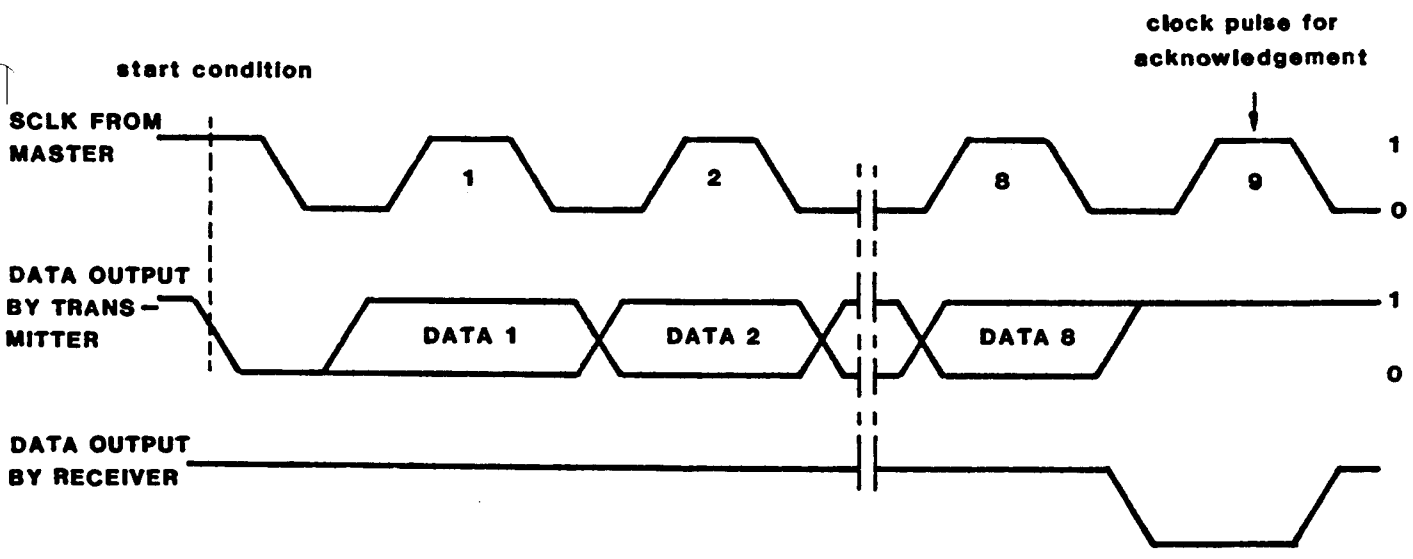


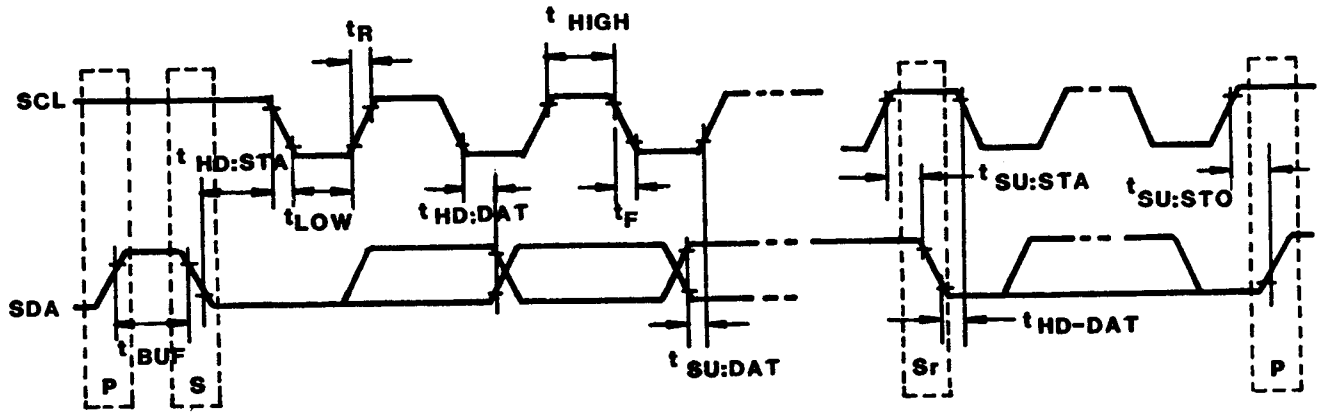
FIGURE 2B ACKNOWLEDGEMENT



ACKNOWLEDGEMENT

An extra clock pulse is generated during which the receiver pulls the data line LOW.

FIGURE 2C I^2C BUS TIMING REQUIREMENTS



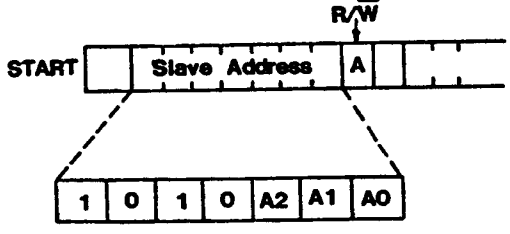
S=START
P=STOP

I^2C BUS PROTOCOL

A thorough description of the inter-IC bus specifications appears in the Philips document number TVE 81107 which is available upon request from General Instrument. The following is a condensed description of each mode of operation.

Chip Address (Slave Address) Allocation: The three chip address inputs of each PCD8582 (A2, A1, A0) must be externally connected to either +5V (V_{DD}) or ground (V_{SS}) thereby assigning to each PCD8582 a unique three-bit chip address. Up to eight PCD8582s may be connected to the I^2C bus. Chip selection is then accomplished through software by setting the least significant three bits of the slave address to the corresponding hardwired logic levels of the selected PCD8582. The correct bus protocol is shown in figure 3.

FIGURE 3 SLAVE ADDRESS ALLOCATION



Erase/Write Mode: In this mode the master transmitter transmits to the PCD8582 slave receiver. Bus protocol is shown in figure 4. Following the START condition and slave address a logic 0 (R/W=0) is placed on the bus and indicates to the addressed device that word address An will follow and is to be written to the on-chip address pointer. The data word to be written to the nonvolatile memory is strobed in next, and is loaded in the address pointer. A second data byte may be strobed in following this the address pointer. In the erase/write mode no more than two successive data bytes may be strobed into the PCD8582. The PCD8582 slave receiver will send an acknowledge bit to the master transmitter after it has received the slave address and again after it has received the word address and each data byte. After the STOP condition the erase/write cycle starts. Its duration is approximately 20ms. if only one byte is written, and 40ms, if two bytes are written.

Read Mode: In this mode the master reads the PCD8582 slave after setting the slave address. See figure 5. Following the write mode control bit (R/W=0) and the acknowledge bit, the word address An is written to the on-chip address pointer.

Next the START condition and slave address are repeated followed by the READ mode control bit (R/W=1). At this point the master transmitter becomes the master receiver and the PCD8582 slave receiver becomes the slave transmitter. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge bit. The PCD8582 slave transmitter will now place the data byte at address A_{n+1} on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to A_{n+2}.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

An alternate READ mode may also be implemented whereby the master reads the PCD8582 slave without first writing to the (voltaile) address pointer. The first address that is read is the last one stored in the pointer. See figure 6.

FIGURE 4 ERASE + REWRITE MODE

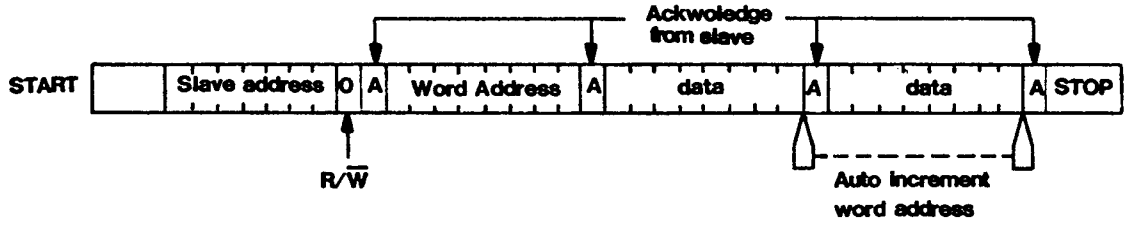


FIGURE 5 READ MODE

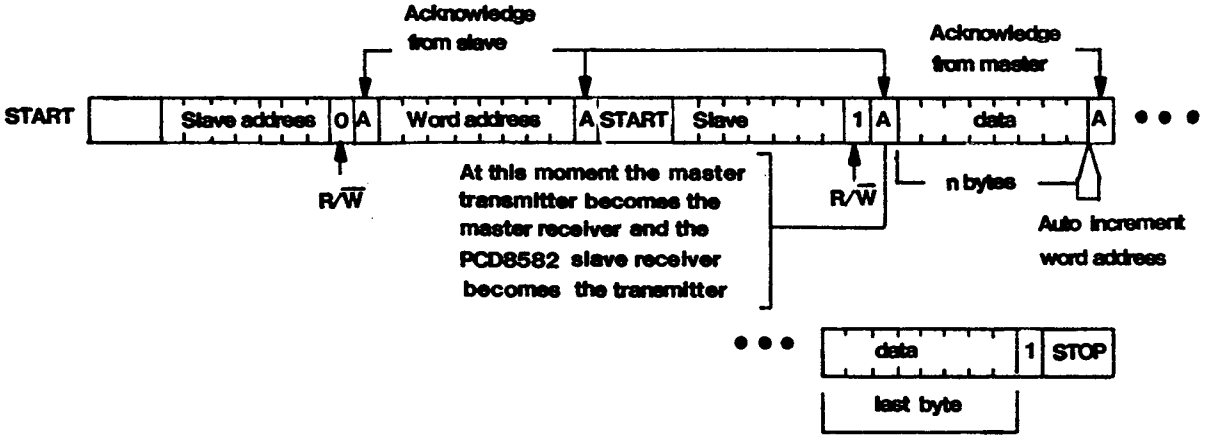
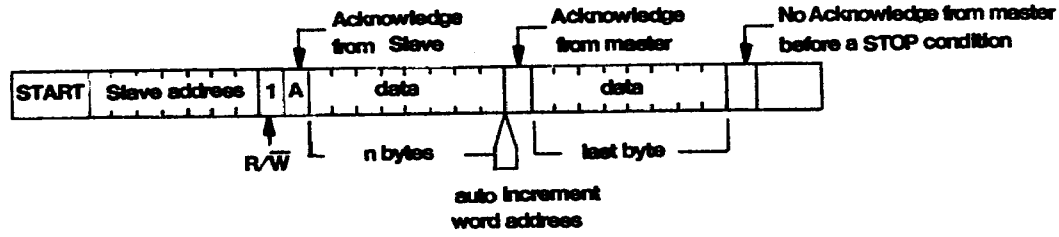
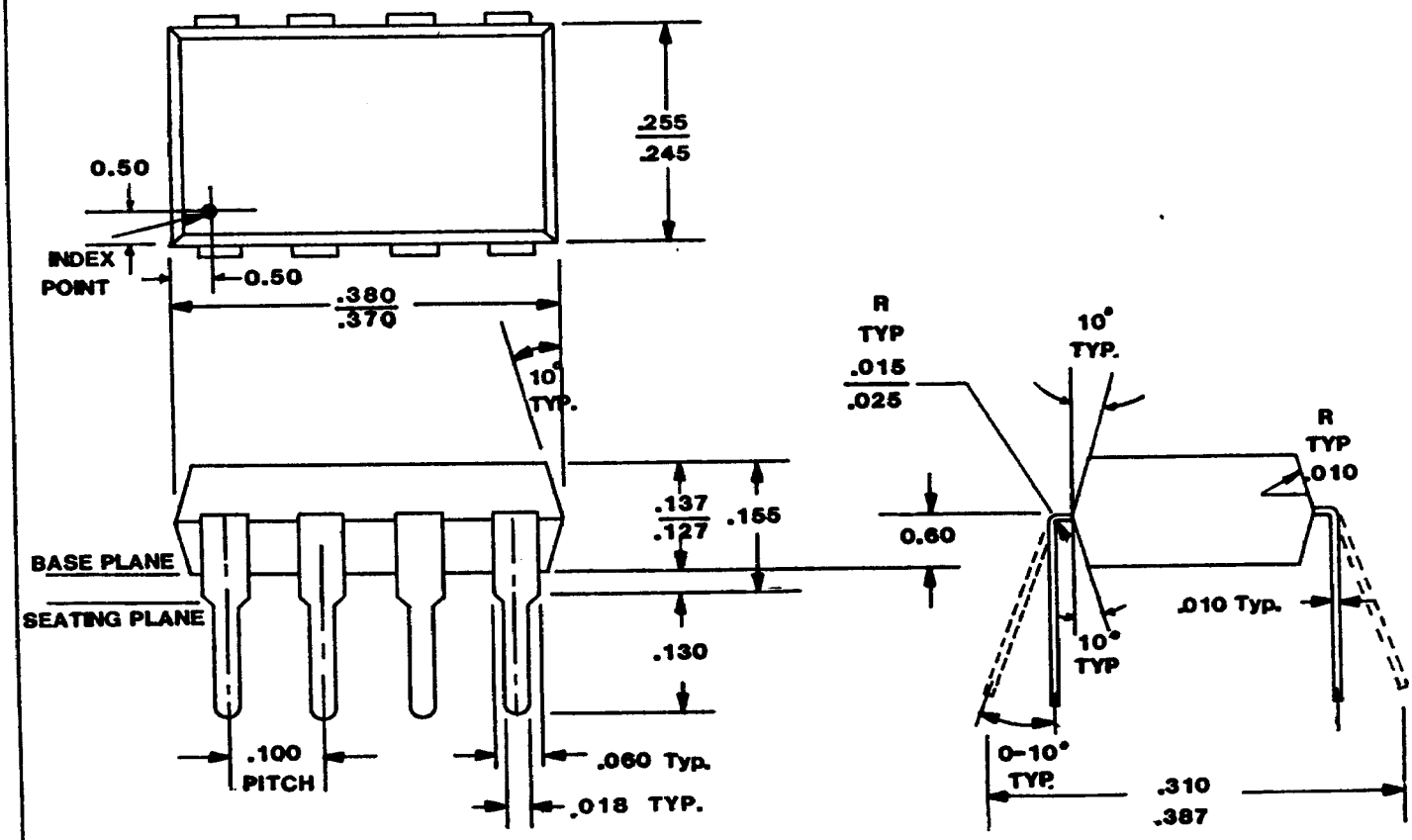


FIGURE 6 ALTERNATE READ MODE



PACKAGE OUTLINE

8 Lead Dual-In-Line (All dimensions are in inches)



NOTE: Unless otherwise specified, all dimensions are ± .002 in.

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