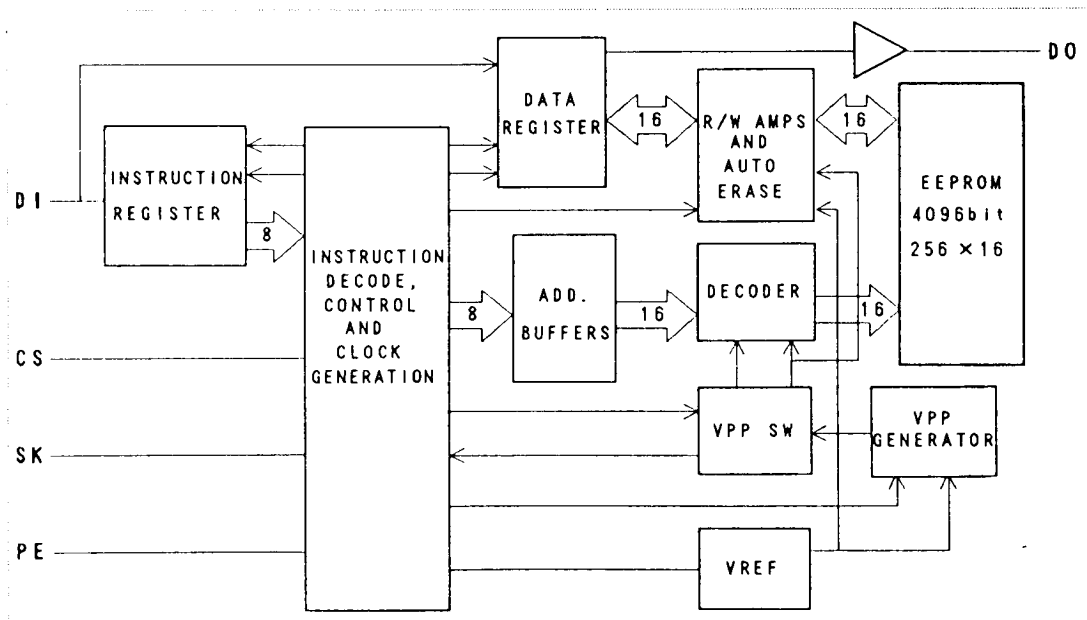


AK93C67 Series

Wide Vcc (2.5V ~ 5.5V) 4096 bit Serial Electrically Erasable PROM

Features

- ADVANCED CMOS E²PROM TECHNOLOGY
- READ/WRITE NON-VOLATILE MEMORY
 - Wide Vcc (2.5V ~ 5.5V) operation
 - 4096 bits, 256 × 16 organization
 - Easy to use yet versatile serial data interface
- LOW POWER CONSUMPTION
 - 5mA Max Active
 - 100 μ A Max Standby, CMOS interface
- SPECIAL FEATURES
 - Automatic write cycle time-out with auto-ERASE
 - Ready/Busy status signal
 - Software and Hardware controlled write protection
- IDEAL FOR LOW DENSITY DATA STORAGE
 - Low cost, space saving, 8-pin package
 - Interfaces with popular microcontrollers and standard microprocessors
- APPLICATION VERSATILITY
 - Alarm Devices, Electronic Locks, Appliances, Terminals, Smart Cards, Satellite Receivers, Meters, Telephones, Tuners, etc.



Block Diagram

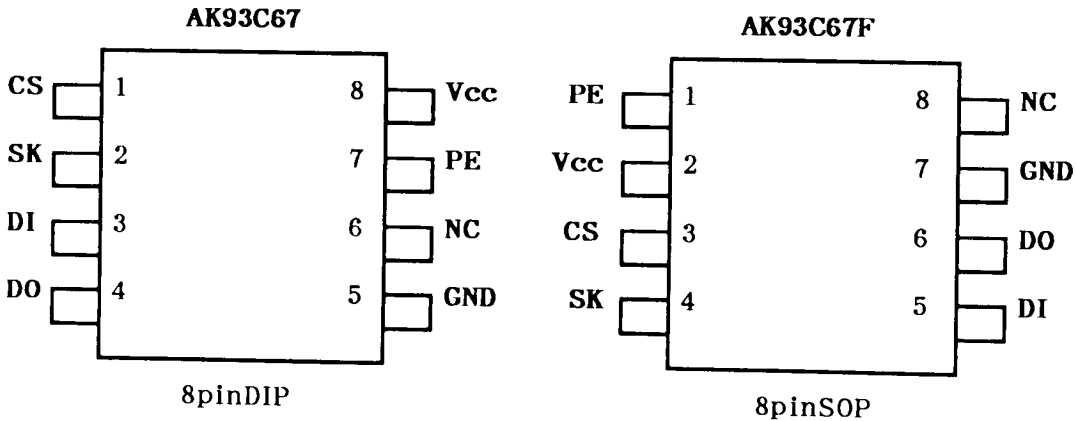
General Description

The AK93C67 is a 4096-bit, serial, read/write, non-volatile memory device fabricated using an advanced CMOS E²PROM technology. Its 4096bits of memory are organized into 256 registers of 16 bits each. It can operate full function under wide operating voltage range from 2.5V to 5.5V. Each register is individually addressable for serial read or write operations. A versatile serial interface, consisting of chip select, clock, program enable, data-in and data-out, can easily be controlled by popular microcontrollers or standard microprocessors. Low power consumption, low cost, and space efficiency make the AK93C67 an ideal candidate for high volume, low density, data storage applications. Special features of the AK93C67 include : automatic write time-out with auto-ERASE, ready/busy status signal, software and hardware controlled write protection and ultra-low standby power mode when deselected (CS=low).

■ **Product Selection Guide**

Model	Temp.Range	Vcc	Package
AK93C67	0°C ~ 70°C	2.5V ~ 5.5V	8pin Plastic DIP
AK93C67F	0°C ~ 70°C	2.5V ~ 5.5V	8pin Plastic SOP

■ **Pin Diagram**



- CS = Chip Select
- SK = Serial Data Clock
- PE = Program Enable
- DI = Serial Data Input
- DO = Serial Data Output
- GND = Ground
- Vcc = Power Supply
- NC = Not Connected

Functional Description

Device Operation

The AK93C67 is a serial 4096 bit peripheral memory device intended for use in non-volatile data storage applications. Its memory organization consists of 256 registers, each 16-bits wide. Each register is independently addressable for read or write operation.

Five 12-bit serial instructions are used to control the operation of the AK93C67. These instructions are serially clocked into the DI input as controlled by the CS, PE and SK input. The instructions include read, erase/write enable, erase/write disable, write and write all. The format of each instruction has a logical "01" as a start bit, two bits as an opcode, and 8 bits of address. During read operations, the DO output is valid as data out after the address is entered. PE (Program Enable) input prevents any accidental programming. PE must be kept high during entering instructions of WRITE, WRAL and EWEN. After a write instruction, the DO output serves as a ready/busy status indicator signaling when the operation is complete allowing further read or write access. The ready/busy status indicator is only valid when CS is active (high). When CS is low, the DO output goes into a high impedance state. After a new instruction is initiated, the DO output also goes to high impedance.

PE input is internally pulled up to Vcc. If PE is left unconnected, the device will accept WRITE, WRAL and EWEN instructions.

CS must be brought low for a minimum of 250ns (Tcs) between consecutive instruction cycles.

During a programming mode (WRITE, WRAL), SK clock is only needed while the actual instruction, i.e. start bit, op-code address and data is being input. It can remain deactivated during the self-timed programming cycle and status check.

Read

The read instruction is the only instruction which outputs serial data on the DO pin. After a read instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out-shift register. A dummy bit (logical "0") precedes the 16-bit data output string. The output data changes during the high states of the system clock.

Erase/Write Enable and Disable

When Vcc is applied to the part, it powers up in the programming disable (EWDS) state. Programming must be preceded by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or Vcc is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is independent of both EWEN and EWDS instructions.

PE must be kept high during entering EWEN instruction.

Write

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data in (DI) pin, CS must be brought low before the next rising edge of the SK clock. PE must be kept high during entering the instruction. This falling edge of CS initiates the self-timed programming cycle. Like programming mode, D0 indicates the ready/busy status of the chip if CS is brought high after a minimum of 250ns(Tcs). D0=logical "0" indicates that programming is still in progress. D0=logical "1" indicates that the register at the address specified in the instruction has been rewritten with the new data pattern specified in the instruction and the part is ready for another instruction. The register to be written into is not necessary to be erased before write operation. DI must be brought low during the self-timed programming cycle and status check. PE must be kept high during entering the instruction.

Write-All

The write-all (WRAL) command writes all registers with the new data pattern specified in the instruction. This command is provided for device evaluation purposes only and is not meant to be used for normal operation. PE must be kept high during entering the instruction.

■ Instruction Set For AK93C67

Instruction	start Bit	Op-code	Address	Data	Comments
READ	01	10	A ₇ -A ₀	D ₁₅ -D ₀ (Output)	READ register
WRITE	01	01	A ₇ -A ₀	D ₁₅ -D ₀ (Input)	WRITE register
EWEN	01	00	11XXXXXX		ERASE/WRITE enable
EWDS	01	00	00XXXXXX		ERASE/WRITE disable
WRAL	01	00	01XXXXXX	D ₁₅ -D ₀ (Input)	Write all registers

AK93C67 has 5 instructions as shown. Note that the Most Significant Bit of any given instruction is a "01" and is viewed as a start bit in the interface sequence. The next 10 bits carry the op-code and the 8-bit address for 1 of 256, 16-bit registers.

■ **ABSOLUTE MAXIMUM RATINGS**

Voltage relative to ground.....-0.6V to +6.0V
 Ambient storage temperature.....-65°C to +125°C
 Lead temperature (soldering 10 sec.).....+260°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

■ **OPERATING CONDITIONS**

Temperature Range 0°C to +70°C
 V_{CC} Power Supply 2.5V ~ 5.5V

■ **NON-VOLATILE CHARACTERISTICS**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T _{DR}	Data Retention Time	Ta=70°C	10			Year
N _{E/W}	Write/Erase Cycles			10 ⁴		Cycle

■ D.C. ELECTRICAL CHARACTERISTICS
 $2.5V \leq V_{CC} \leq 5.5V, 0^\circ C \leq T_a \leq 70^\circ C$

Symbol	Parameter	Conditions	Min.	Max.	UNIT
I_{CC}	Operating Current TTL/CMOS Inputs	DO=OPEN, CS=PE= V_{IH} $V_{CC}=5.5V, f=1MHz$		5	mA
I_{CCSB1}	Standby Current CMOS Inputs	$V_{CC}=5.5V, CS=V_{IL}$ Inputs= V_{CC} orGND DO=OPEN		100	μA
V_{IL1}	Input Voltage Low 1	$4.5V \leq V_{CC} \leq 5.5V$	-0.1	0.8	V
V_{IL2}	Input Voltage Low 2	$V_{CC}=2.5V$	-0.1	0.6	V
V_{IH1}	Input Voltage High 1	$4.5V \leq V_{CC} \leq 5.5V$	2.0	$V_{CC}+1$	V
V_{IH2}	Input Voltage High 2	$V_{CC}=2.5V$	1.8	$V_{CC}+1$	V
V_{OL}	Output Voltage Low	$I_{OL}=2.1mA$		0.4	V
V_{OH1}	Output Voltage High 1	$I_{OH}=0.4mA$ $4.5V \leq V_{CC} \leq 5.5V$	2.2		V
V_{OH2}	Output Voltage High 2	$I_{OH}=0.4mA, V_{CC}=2.5V$	1.8		V
I_{L1}	Input Leakage Current	$V_{IN}=5.5V$		10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=5.5V, CS=0V$		10	μA

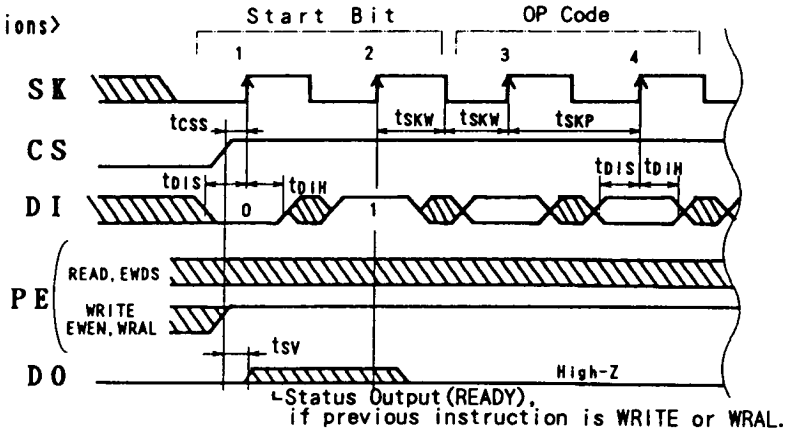
 AK93C67 is TTL compatible under $V_{CC}=4.5V \sim 5.5V$.

■ A.C. ELECTRICAL CHARACTERISTICS
 $2.5V \leq V_{CC} \leq 5.5V, 0^{\circ}C \leq T_a \leq 70^{\circ}C$

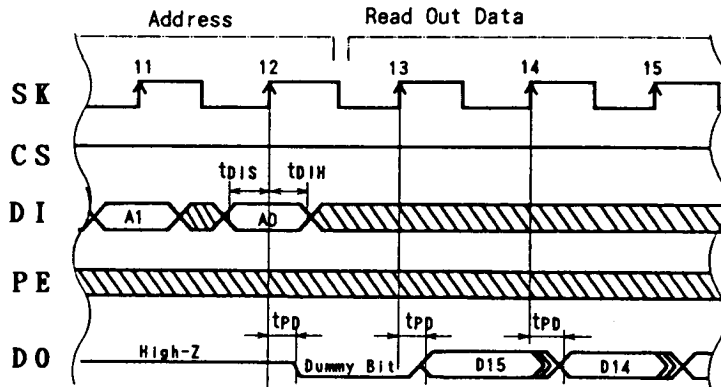
Symbol	Parameter	Conditions	Min.	Max.	UNIT
t_{SKP1}	SK Cycle Time 1	$4.5V \leq V_{CC} \leq 5.5V$	1		μs
t_{SKP2}	SK Cycle Time 2	$V_{CC}=2.5V$	4		μs
t_{SKW1}	SK Pulse Width low/high1	$4.5V \leq V_{CC} \leq 5.5V$	500		ns
t_{SKW2}	SK Pulse Width low/high2	$V_{CC}=2.5V$	1		μs
t_{CSS}	CS Setup Time		100		ns
t_{CSH}	CS Hold Time		0		ns
t_{DIS}	Data Setup Time		200		ns
t_{DIH}	Data Hold Time		200		ns
t_{PD}	SK to DO Delay	$C_L=100pF,$ $V_{OL}=0.8V, V_{OH}=2.0V$ $V_{IL}=0.45V, V_{IH}=2.4V$		500	ns
$t_{E/W}$	Selftimed Program Cycle			15	ms
t_{CS}	Min CS Low Time		250		ns
t_{SV}	CS to Status Valid	$C_L=100pF$		500	ns
t_{OH}/t_{IH}	CS to Output High-Z			100	ns

■ AC WAVEFORM □ Instruction Timing

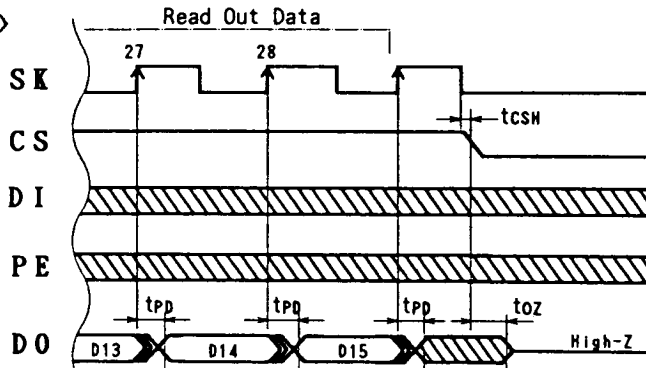
<The Start of instructions>



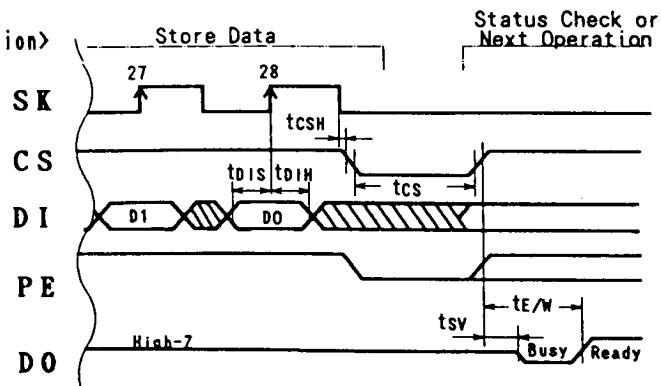
< The Read Out Data >



<The End of READ instruction>

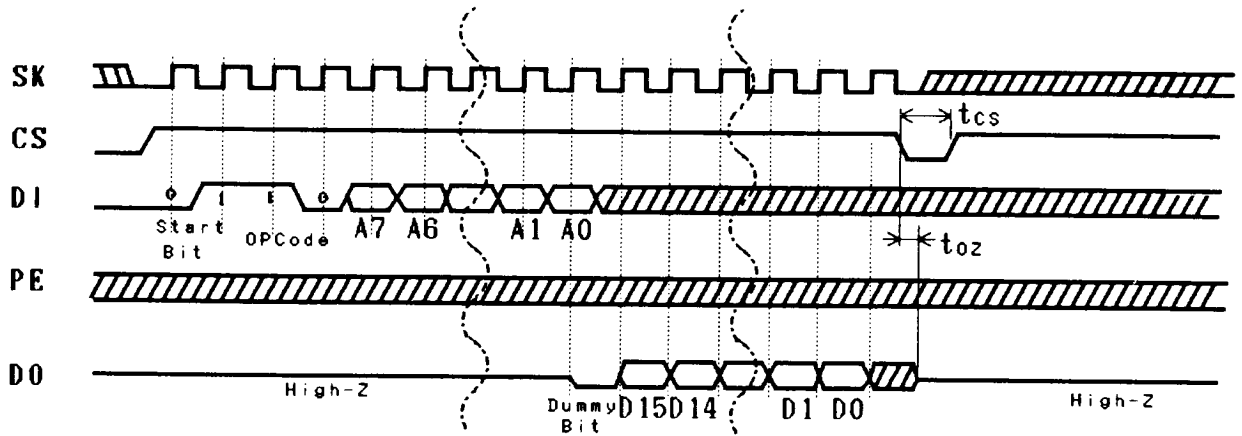


<The End of WRITE, WRAL instruction>

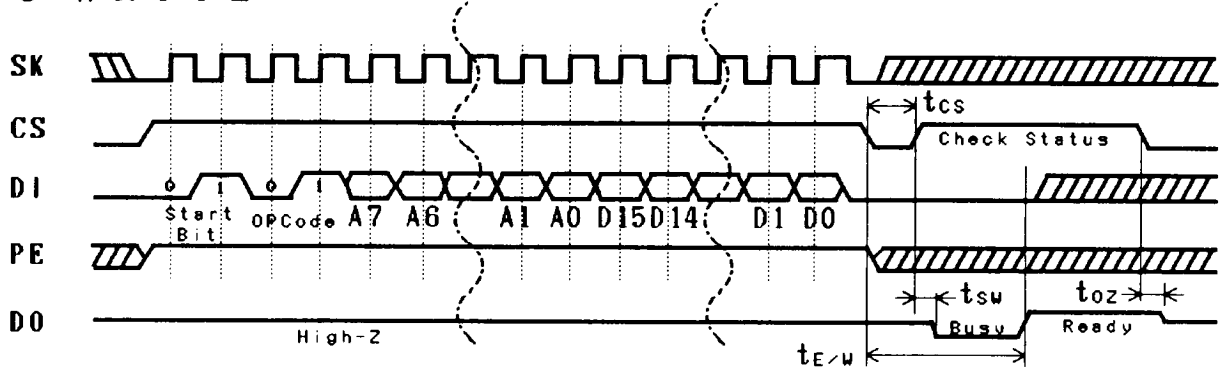


■ AC WAVEFORM □ Synchronous Data timing

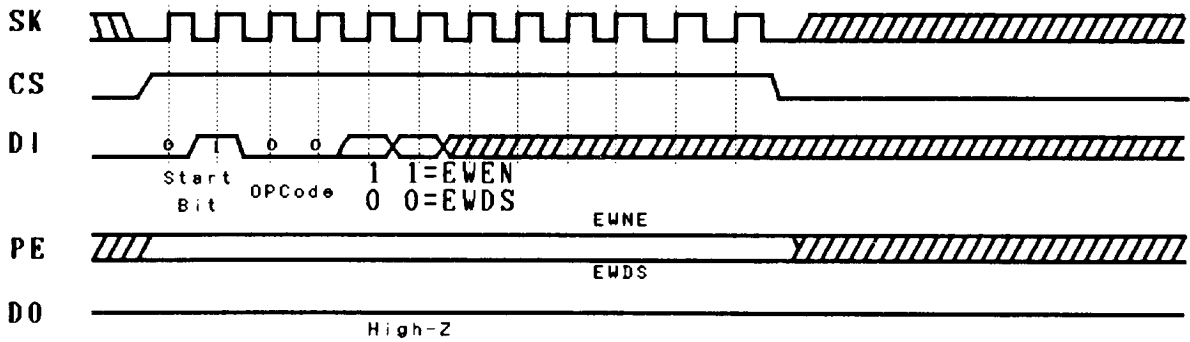
● READ



● WRITE



● EWEN / EWDS



● WRAL

